L Number	Hits	Search Text	DB	Time stamp
1	1793	257/379,380,408,536.ccls.	USPAT; US-PGPUB	2003/05/21 13:37
3	83	mosfet and (print adj head)	USPAT; US-PGPUB	2003/05/21 13:50
4	80	(mosfet and (print adj head)) and @ad<=20020118	USPAT; US-PGPUB	2003/05/21 13:42
5	13666	print adj head	USPAT; US-PGPUB	2003/05/21 13:41
6	4503	(print adj head) and substrate	USPAT; US-PGPUB	2003/05/21 13:42
7	148	((print adj head) and substrate) and (doping or implanting)	USPAT; US-PGPUB	2003/05/21 13:42
8	136	(((print adj head) and substrate) and (doping or implanting)) and @ad<=20020118	USPAT; US-PGPUB	2003/05/21 13:54
9	83	((((print adj head) and substrate) and (doping or implanting)) and @ad<=20020118) and (hole or opening or recess or recess or trench)	USPAT; US-PGPUB	2003/05/21 13:43
10	70	(((((print adj head) and substrate) and (doping or implanting)) and @ad<=20020118) and (hole or opening or recess or recess or trench)) and contact	USPAT; US-PGPUB	2003/05/21 13:54
11	25	mosfet and (print adj cartridge)	USPAT; US-PGPUB	2003/05/21 13:55
12	25	(mosfet and (print adj cartridge)) not ((((((print adj head) and substrate) and (doping or implanting)) and @ad<=20020118) and (hole or opening or recess or recess or trench)) and contact)	USPAT; US-PGPUB	2003/05/21 13:47
13	2	mosfet and (print adj cartridge)	EPO; JPO; DERWENT; IBM_TDB	2003/05/21 13:49
14	20	mosfet and (print adj head)	EPO; JPO; DERWENT; IBM_TDB	2003/05/21 13:50
15	20	(mosfet and (print adj head)) not (mosfet and (print adj cartridge))	EPO; JPO; DERWENT; IBM_TDB	2003/05/21 13:53
17	1641	347/54,57-59,63,65.ccls.	USPAT; US-PGPUB	2003/05/21 13:54
18	1536	347/54,57-59,63,65.ccls. and @ad<=20020118	USPAT; US-PGPUB	2003/05/21 14:03
19	1070	(347/54,57-59,63,65.ccls. and @ad<=20020118) and contact	USPAT; US-PGPUB	2003/05/21 13:55
20	26	mosfet and ((347/54,57-59,63,65.ccls. and @ad<=20020118) and contact)	USPAT; US-PGPUB	2003/05/21 13:59
22	708	mosfet and ((electrical adj contact$1) same (hole or opening or recess or via))	USPAT; US-PGPUB	2003/05/21 14:01
23	1639	mosfet and ((electrical adj contact$1) same (source or drain or gate or electrode))	USPAT; US-PGPUB	2003/05/21 14:03
24	1326	mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))	USPAT; US-PGPUB	2003/05/21 14:03
25	1235	(mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118	USPAT; US-PGPUB	2003/05/21 14:03
26	749	((mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118) and dielectric	USPAT; US-PGPUB	2003/05/21 14:04
27	740	(((mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118) and dielectric) and (gate or electrode)	USPAT; US-PGPUB	2003/05/21 14:04
28	494	((((mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118) and dielectric) and (gate or electrode)) and (substrate with p)	USPAT; US-PGPUB	2003/05/21 14:05

29	379	(((((mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118) and dielectric) and (gate or electrode)) and (substrate with p)) and (doping or implanting)	USPAT; US-PGPUB	2003/05/21 14:05
30	319	((((((mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118) and dielectric) and (gate or electrode)) and (substrate with p)) and (doping or implanting)) and (n with dop$3)	USPAT; US-PGPUB	2003/05/21 14:06
31	267	((((((mosfet and ((electrical adj contact$1) with (source or drain or gate or electrode))) and @ad<=20020118) and dielectric) and (gate or electrode)) and (substrate with p)) and (doping or implanting)) and (n with (source or drain))	USPAT; US-PGPUB	2003/05/21 14:19
33	1015	438/$.ccls. and print	USPAT; US-PGPUB	2003/05/21 14:20
34	1015	438/$.ccls. and print	USPAT; US-PGPUB	2003/05/21 14:20
35	98	438/$.ccls. and (print adj head)	USPAT; US-PGPUB	2003/05/21 14:24

US-PAT-NO: 6492678

DOCUMENT-IDENTIFIER: US 6492678 B1

TITLE: High voltage MOS transistor with gate extension

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Detailed Description Text - DETX (9):

Selective masking and etching may then be performed to remove a portion of dielectric 122 to form opening 125 as shown in FIG. 2E. Opening 125 in dielectric 122 provides a window through which gate layers 116 and 124 come into **electrical contact** with each other. Opening 125 divides dielectric 122 into portions of 122A and 122B. Second gate layer 124 may then be formed over opening 125 and portions 122A and 122B of the dielectric as shown in FIG. 2E. Second gate layer 124 may be formed, for example, by blanket deposition and doping followed by selective masking and etching. Second gate layer 124 may be formed of any suitable conductive material such as polysilicon, polycide, silicide, or refractory metal (such as Tantalum or Molybdenum). Gate layer 124 may, for example, have a thickness of 2500 angstroms. Gate layers 116 and 124 physically contact each other through opening 125 so that they are electrically coupled together. Layers 124 and 116 form the gate of the MOS transistor. Care should be taken in ensuring no residual portions of the material used to form second gate layer 124 are adjacent to first gate layer 116, other than through opening 125.

US-PAT-NO: 6215155

DOCUMENT-IDENTIFIER: US 6215155 B1

TITLE: Silicon-on-insulator configuration which is compatible with bulk CMOS architecture

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Detailed Description Text - DETX (10):

FIG. 4 shows the resistances, capacitances and the depletion zone formed under an N-channel MOSFET in the architecture according to the invention. As before, the N-channel MOSFET, generally indicated by the numeral 90 includes a polycrystalline silicon gate 92, a N.sup.+ source region 94, and a N.sup.+ drain region 96. Between the source region 94 and the drain region 96, and below the gate 92, a P.sup.- body region 98 is provided. **Electrical contact to the source** region 94, the gate region 96 and the gate 92, is made respectively by a metal source electrode 100, a metal drain electrode 102, and a metal gate electrode 104, which penetrate through an interoxide layer 105. Also provided is a metal P-well contact electrode 106. Surrounding the various semiconductor regions below the interoxide layer 105 is a field oxide layer 107. Also as before, a buried oxide layer 108 is present below the P.sup.- body region 98. Located below the buried oxide layer 108 and below the P.sup.- body region 98 is a region 112, which is of the same conductivity type i.e. P as the channel region 98. In the illustrated MOSFET 90, the region 110 is part of a P-well 112 which is formed above and below i.e. divided by the

buried oxide layer 108.
The P-well is formed in an N type substrate 114 using a bulk CMOS P-well mask
as described with reference to FIG. 3. A depletion zone 116 forms between the
P-well 112 and the N-substrate 114, which serves to reduce charge transfer due
to displacement current induced in the substrate 114 by electrode signals
applied to the N.sup.+ regions 94, 96, and interconnect 106. Since active
devices are not placed in the P-well 112, below the buried oxide layer 108, the
doping levels of the P-well 112 in this region, and of the substrate 114, may
be very light, less than or approximately equal to 1.0E15 atoms/cc. This
results in a depletion spread i.e. the size of the depletion zone 116 of
approximately 1 .mu.m, or greater, for very lightly doped P-well/N-substrate
junctions. The capacitance 118 resulting from the depletion zone 116, together
with the buried oxide layer capacitance 120, which are in series as shown,
reduces the capacitance between the electrodes 100, 102, 106 and the
N-substrate 114.